47. (Added)

A semiconductor device comprising:

a semiconductor region formed on a semiconductor substrate;

a plurality of field effect transistors formed in said semiconductor region; and

a power supply wiring for supplying a power supply voltage to a plurality of said field effect transistors,

wherein at least one of a pair of semiconductor regions for source and drain of unused field effect transistor among a plurality of said field effect transistors and said power supply wiring are electrically connected.

48. (Added)

A semiconductor device comprising:

a semiconductor region formed on a semiconductor substrate;

a plurality of basic cells regularly arranged on said semiconductor substrate;

a plurality of field effect transistors arranged in each of a plurality of said basic cells and formed in said semiconductor region; and

a power supply wiring for supplying a power supply voltage to a plurality of said field effect transistors,

wherein at least one of a pair semiconductor regions for source and drain of unused field effect transistors among a plurality of said basic cells and

said power supply wiring are electrically connected.

49. (Added)

A semiconductor device according to claim 48, wherein said unused field effect transistors are included in unused basic cells.

50. (Added)

A semiconductor device comprising:

a semiconductor region formed on a semiconductor substrate;

a plurality basic cells regularly arranged in each of a plurality of said basic cells and formed in said semiconductor region;

a power supply wiring for supplying a power supply voltage to a plurality of said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wiring,

wherein a plurality of said switch elements are discretely arranged within said semiconductor region, and

wherein said switch element or logic circuit is constituted by said basic cells.

51. (Added)

A semiconductor device according to claim 50, wherein logic circuits are constituted by said discretely arranged switch elements and the basic cells formed among said switch elements.

52. (Added)

A semiconductor device according to claim 50 or 51, wherein at least one of a pair of semiconductor regions for source and drain of unused field effect transistors among a plurality of said basic cells and said power supply wiring are electrically connected.

53. (Added)

A semiconductor device according to claim 52, wherein said unused field effect transistors are included in unused basic cells.

54. (Added)

A semiconductor device comprising:

a semiconductor region formed on a semiconductor substrate;

a plurality of basic cells regularly arranged on said semiconductor substrate;

a plurality of field effect transistors arranged in each of a plurality of said basic cells and formed in said semiconductor region;

a power supply wiring for supplying the power supply voltage to a plurality of said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wiring,

wherein said switch elements are discretely arranged in said semiconductor region, and

wherein said basic cell is formed of the field

effect transistors same as those structuring logic circuits in such a manner as forming said switch elements.

55. (Added)

A semiconductor device according to claim 54, wherein at least one of a pair of semiconductor regions for source and drain of unused field effect transistors among a plurality of said basic cells and said power supply wiring are electrically connected.

56. (Added)

A semiconductor device according to claim 55, wherein said unused field effect transistors are included in unused basic cells.

57. (Added)

A semiconductor device comprising:

a semiconductor region formed on a semiconductor substrate;

a plurality of basic cells regularly arranged on said semiconductor substrate;

a plurality of field effect transistors arranged in each of a plurality of said basic cells and formed on said semiconductor region;

a power supply wiring for supplying the power supply voltage to a plurality of said field effect transistors; and

switch elements provided between said semiconductor region and said power supply wiring,

wherein said switch elements are constituted by the field effect transistors of said basic cells,

wherein said switch elements are discretely arranged within said semiconductor region, and

wherein logic circuits are constituted by said discretely arranged switch elements and the basic cells formed among the switch elements.

58. (Added)

A semiconductor device according to claim 57, wherein at least one of a pair of semiconductor regions for source and drain of unused field effect transistors among a plurality of said basic cells and said power supply wiring are electrically connected.

59. (Added)

A semiconductor device according to claim 58, wherein said unused field effect transistors are included in unused basic cells.